

FIG. 1

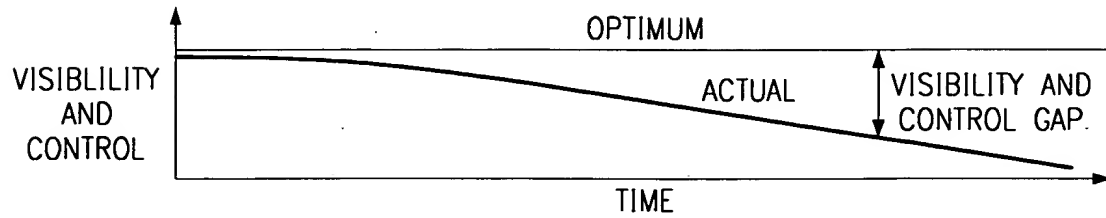


FIG. 2

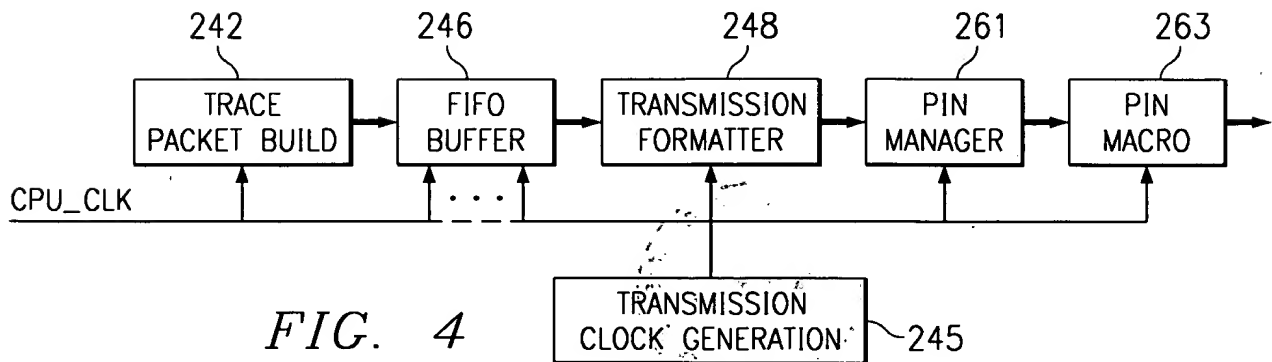
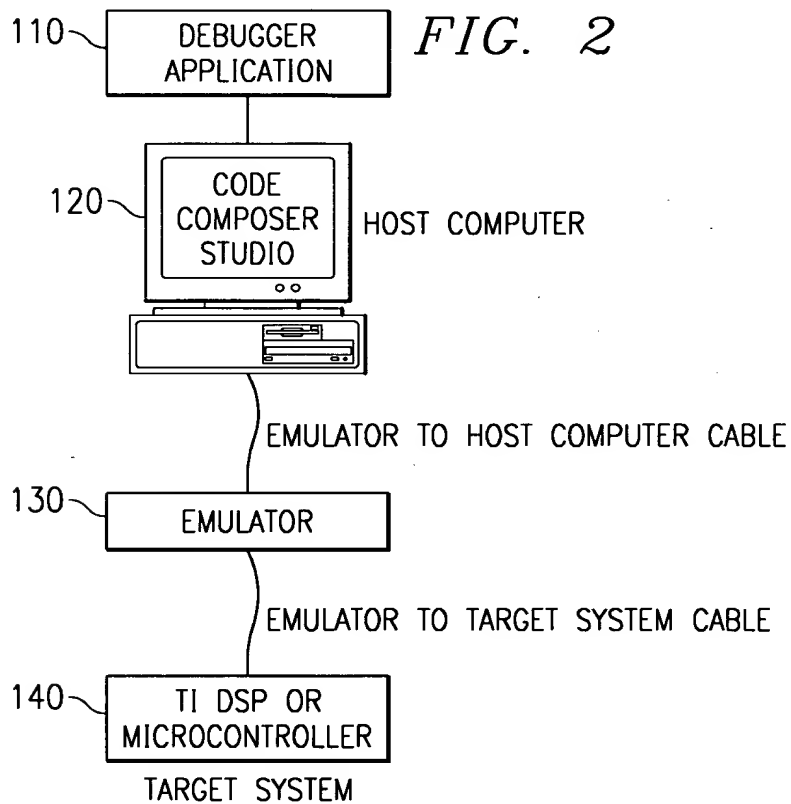


FIG. 4

FIG. 3

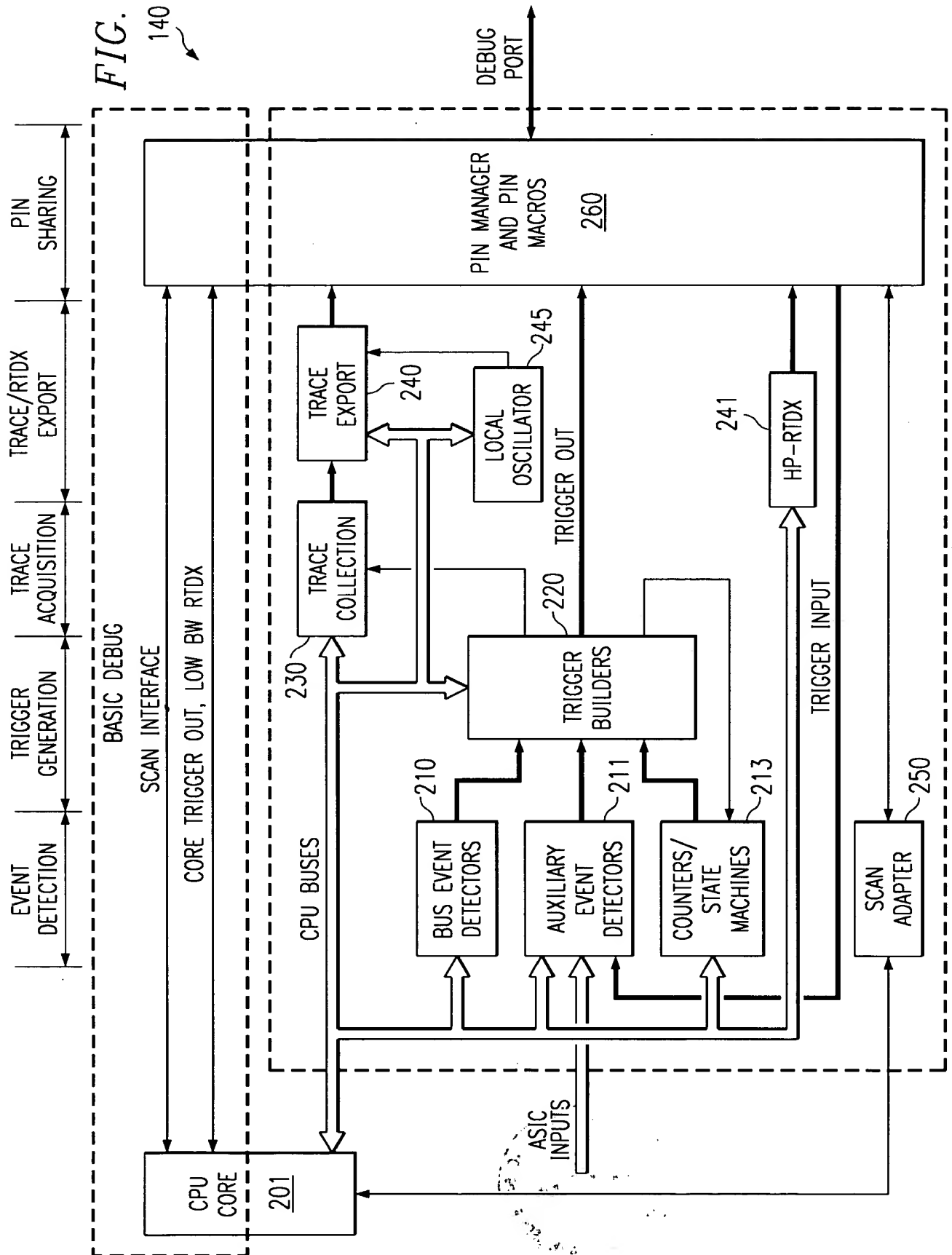


FIG. 5

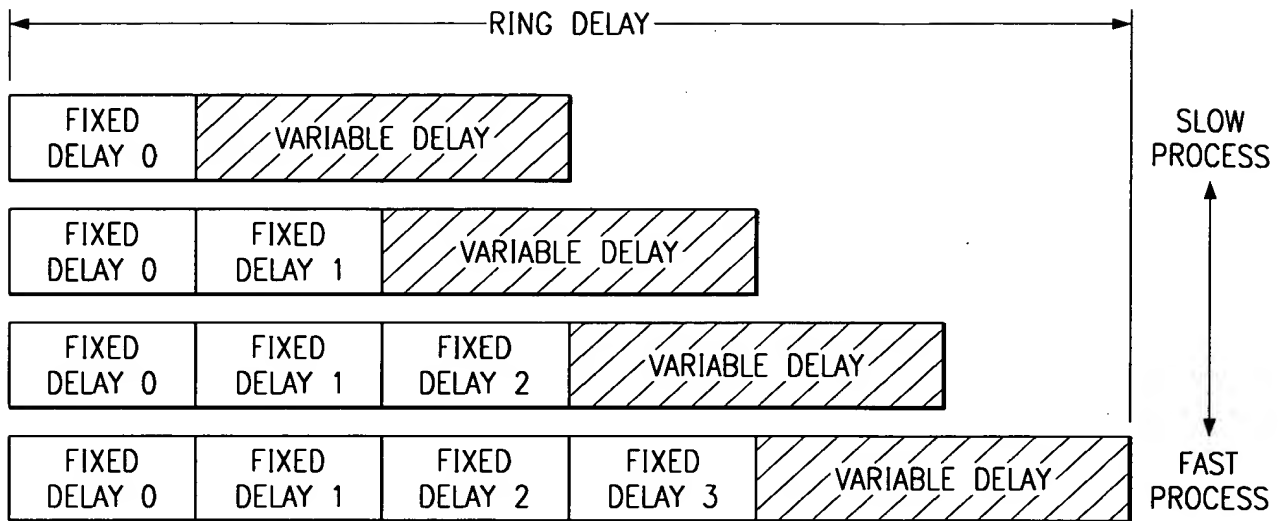
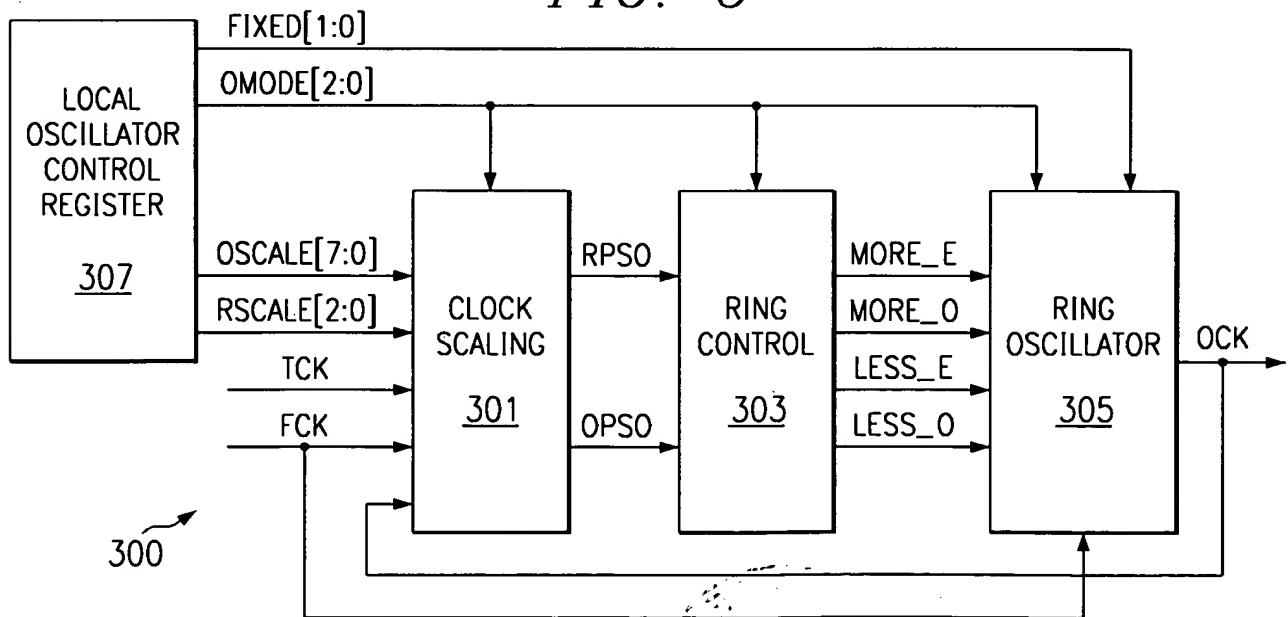


FIG. 6



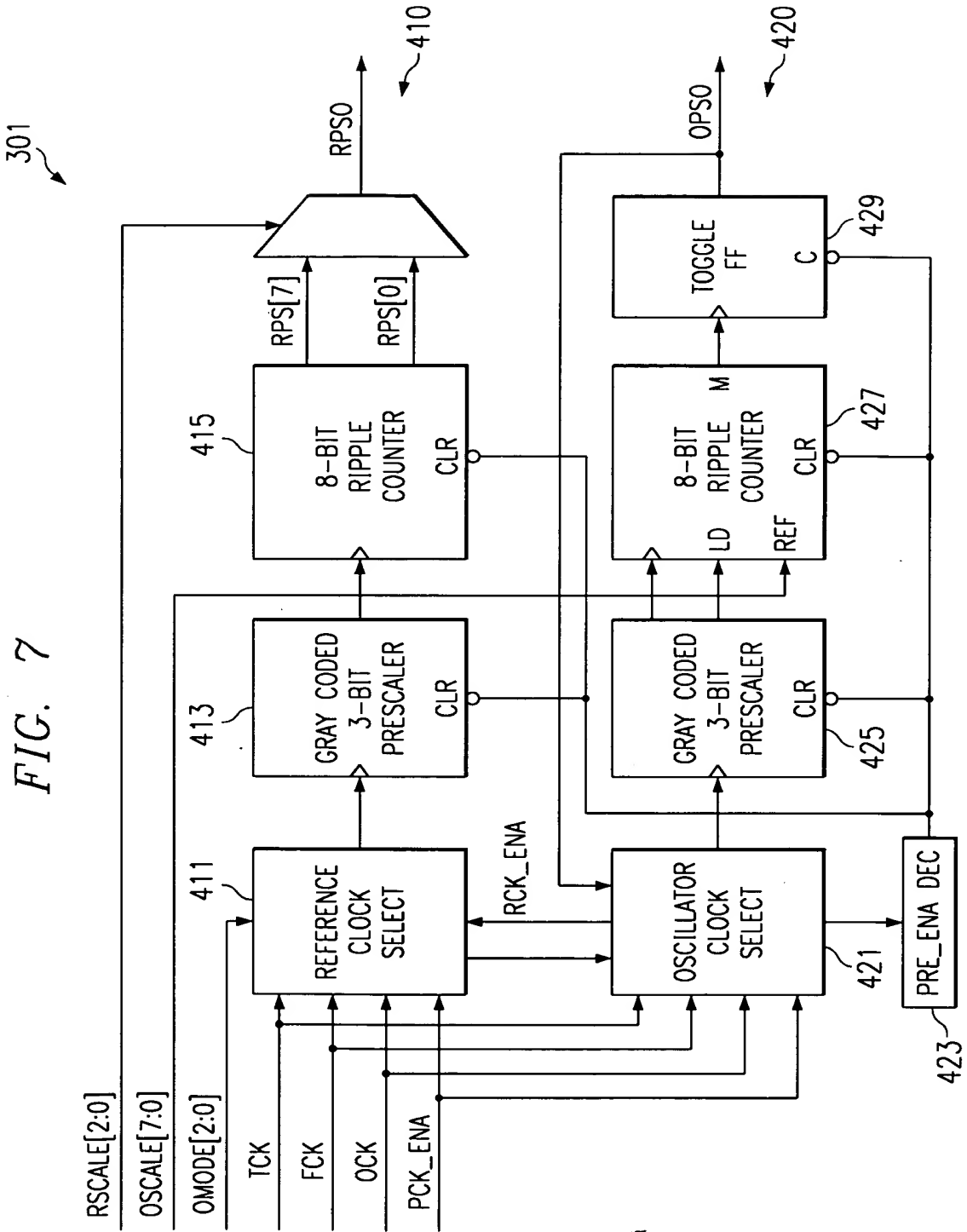


FIG. 8

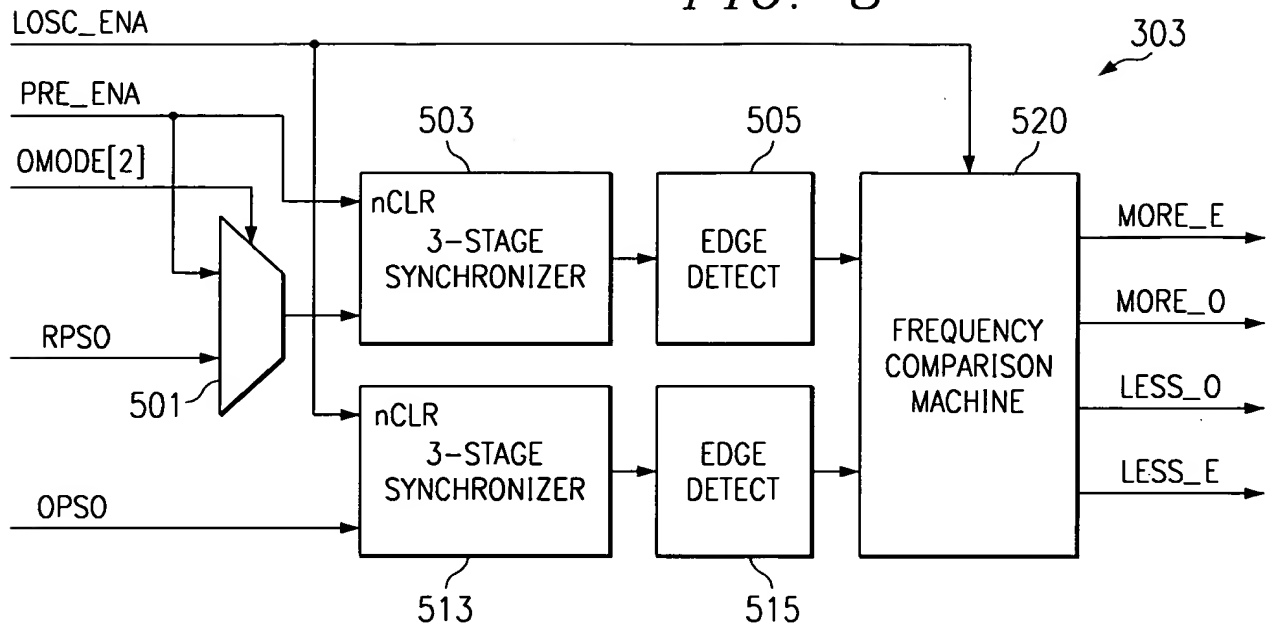
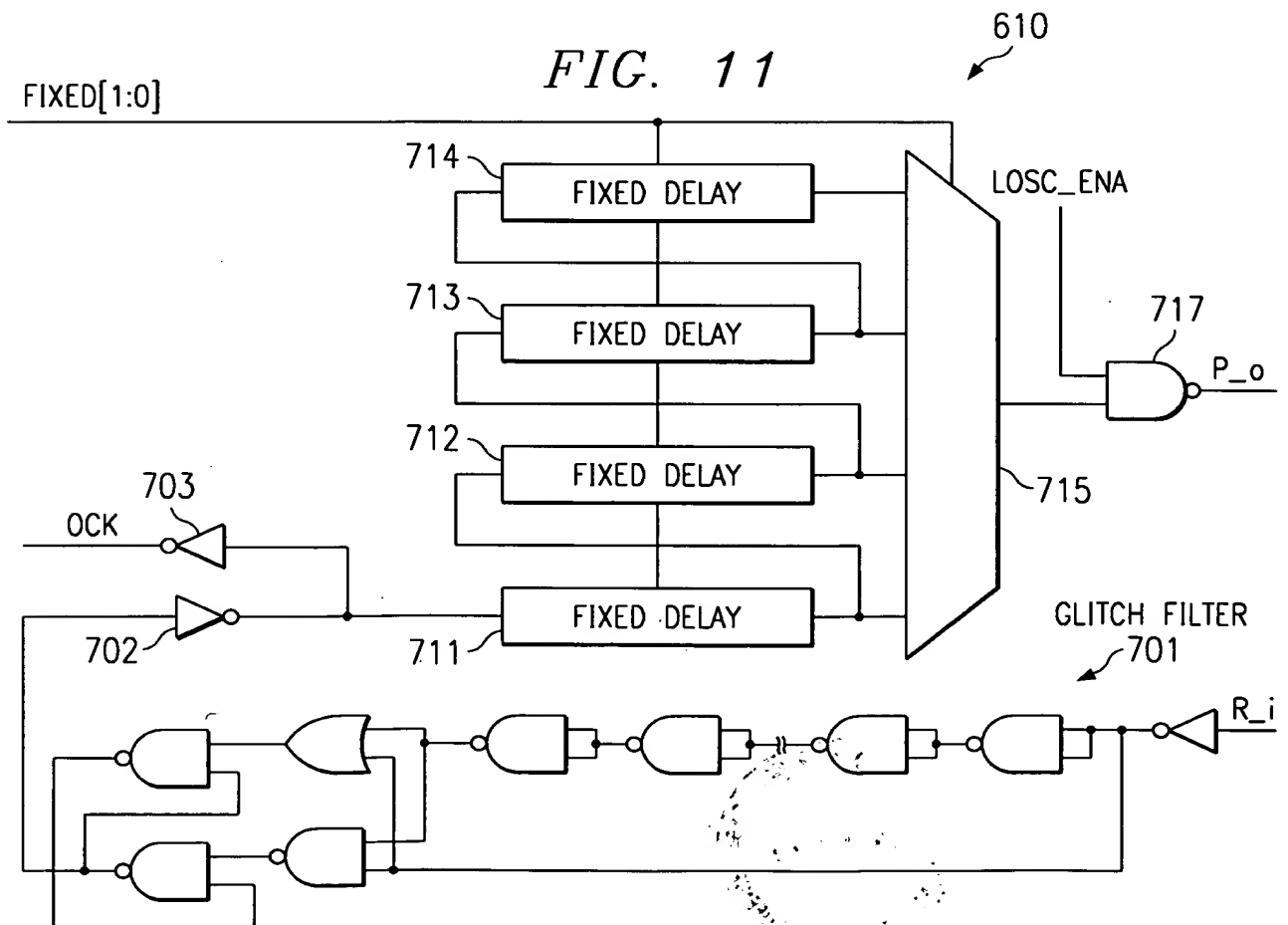
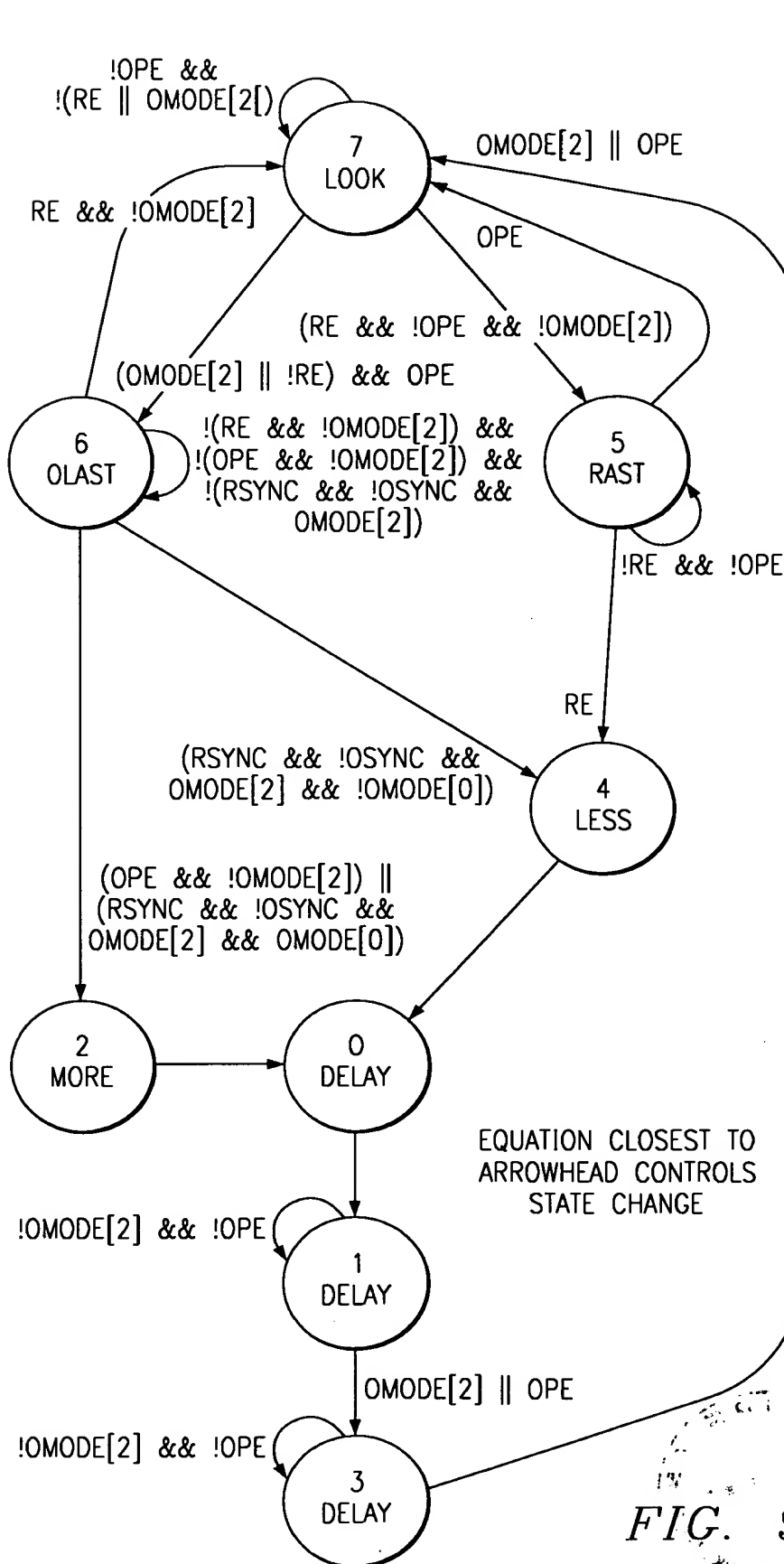


FIG. 11





# SIGNAL DEFINITION

RE - REFERENCE EDGE  
OPE - OSCILLATOR  
POSITIVE EDGE  
RSYNC - REFERENCE  
INPUT SYNCHRONIZED  
OSYNC - OSCILLATOR  
INPUT SYNCHRONIZED

## STATE FUNCTION (OMODE[2] == FALSE)

- 0 - DELAY OR START STATE
- 1 - WAIT FOR OSCILLATOR  
PRESCALER POSITIVE EDGE
- 2 - OSCILLATOR FASTER  
THAN REFERENCE
- 3 - WAIT FOR OSCILLATOR  
PRESCALER CARRY EDGE
- 4 - REFERENCE FASTER  
THAN OSCILLATOR
- 5 - REFERENCE EDGE
- 6 - OSCILLATOR EDGE
- 7 - WAIT FOR OSCILLATOR  
OR REFERENCE EDGE

## STATE FUNCTION (OMODE[2] == TRUE)

- 0 - WAIT FOR  
PRE\_ENA (RSYNC)
- 1 - DELAY
- 2 - INCREASE RING DELAY
- 3 - DELAY
- 4 - DECREASE RING DELAY
- 5 - ILLEGAL
- 6 - END OF MEASUREMENT,  
WAIT FOR OPSO TO GO  
TO ZERO (!OSYNC) AND  
RSYNC TO GO TO  
A ONE (PRE\_ENA)
- 7 - OPSO TO GO TO ONE

LOSC\_ENA ASYNCHRONOUSLY  
ASSIGNS THE STATE TO 0  
WHEN A LOGIC 0

FIG. 9

$$CKENA = !OMODE[2] \parallel STATE[7]$$

